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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/510,385

10/06/2004

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62790(4590-340)

6495

33308 7590 02/13/2008
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EXAMINER

NGUYEN, THANH T

ART UNIT

PAPER NUMBER

2813

MAIL DATE

DELIVERY MODE

02/13/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/510,385	Applicant(s) LEFORT ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 9-21 is/are pending in the application.
- 4a) Of the above claim(s) 12-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-11 and 19-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1- 7, 9-11, 19-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4-7, 10-11, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (U.S. Patent No. 2002/0047188) figures 3-4 in view of Martin et al. (U.S. Patent No. 2002/0047188) figures 6-7.

Referring to figures 3-4, teaches process of fabricating a microstructure having a vacuum cavity, comprising the following steps:

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a) producing, in the thickness of a first silicon wafer (10, called boron doped wafer, paragraph# 30), a porous silicon region intended to format least a part of one wall of the cavity and capable of absorbing residual gases in the cavity (see paragraph# 31);

b) joining the first silicon wafer (10) to a second wafer (50, called silicon cap), so as to produce the cavity (see figure 2, 4).

Regarding to claim 4, wherein prior to step b), the process includes a step of carrying out a physico-chemical preparation of the surfaces of the wafers used in step b) (see paragraph# 30).

Regarding to claim 5, wherein prior to step b), the process includes a step of outgasing the wafers used in step b) (see paragraph# 31).

Regarding to claim 6, wherein the joining operation of step b) is carried out under vacuum (see paragraph# 38).

Regarding to claim 7, wherein the joining operation is carried out by bonding at ambient Temperature (see paragraph# 34).

Regarding to claim 10, wherein the second wafer and/or the intermediate wafer are made of silicon or glass (see paragraph# 28).

Regarding to claim 11, wherein the process is applied collectively to several Microstructures (called micromachined devices, see paragraph# 5).

Regarding to claim 19, wherein the joining is carried out by brazing (see paragraph# 34, it is noted that annealing process would carried out by brazing).

However, the first embodiment does not clearly teach the bonding process at a specific temperature.

Martin et al. teaches in figure 6-7, bonding the wafer to the silicon cap layer by using a temperature of at least about 385⁰C (see paragraph# 34).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the temperature range, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.-annealing between 400 and 1000 degrees Celsius), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- annealing between 400 and 1000 degrees Celsius) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form bond the wafers together by using anneal process in process Martin et al. because the process is known in the semiconductor art to bond the wafers together.

Claims 2, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (U.S. Patent No. 2002/0047188) figures 3-4 in view of Martin et al. (U.S. Patent No.

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2002/0047188) figures 6-7 as applied to claims 1, 4-7, 10-11, 19 above in view of Najafi et al. (U.S. Patent No. 6,499,354).

Martin et al. teaches a method of forming a porous silicon layer (getter) on the silicon wafer. However, the reference does not teach impregnate the layer with titanium material.

Najafi et al. teaches a method of impregnate the region (called getter, 2) with another material (titanium, see col. 4, lines 35-44).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to impregnate the region (called getter, 2) with another material (titanium) in process of Martin et al. as taught by Najafi et al. because the process is known in the semiconductor art to eliminate gases created during attachment inside micromachine vacuum cavities.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (U.S. Patent No. 2002/0047188) figures 3-4 in view of Martin et al. (U.S. Patent No. 2002/0047188) figures 6-7 as applied to claims 1, 4-7, 10-11, 19 above in view of Wood (U.S. Patent No. 5,861,545).

Martin et al. teaches a method of joining two wafers together. However, the reference does not teach the cavity has a predetermined height, the joining operation of step b) is carried out by means of an intermediate wafer whose thickness contributes to the height of the cavity.

Wood teaches in figure 3, forming a first wafer (83), second wafer (87), and the intermediate wafer (called spacer, 86).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form an intermediate wafer between the upper and the lower wafer in process of Martin et al. as taught by Wood because intermediate wafer would help to join the upper wafer to the lower wafer and as well as to define the thickness of the cavity between the wafer.

Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (U.S. Patent No. 2002/0047188) figures 3-4 in view of Martin et al. (U.S. Patent No. 2002/0047188) figures 6-7 as applied to claims 1, 4-7, 10-11, 19 above in view of Benzel et al. (U.S. Patent No. 7,037,438).

Martin et al. teaches a method of forming a porous silicon region and annealing the porous silicon region.

However, the reference does not teach annealing step, the porous silicon region is activated allowing a surface of the porous silicon layer to be cleaned by desorption of H molecules present after production of the porous silicon region.

Benzel et al. teaches annealing step, the porous silicon region is activated allowing a surface of the porous silicon layer to be cleaned by desorption of H molecules present after production of the porous silicon region(see claim 21).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would anneal to clean the porous silicon layer by desorption of H molecules in process of Martin et al. as taught by Benzel et al. because desorption hydrogen

molecules from the porous layer is known in the art to form a layer free of hydrogen as well as other species from the porous surface.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pairdirect.uspto.gov>. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Thanh Nguyen
Primary Examiner, Art Unit 2813

TTN